MRS Advances
https://doi.org/10.1557/s43580-022-00412-1

ORIGINAL PAPER

Introducing the Purion H200™ single wafer high current implanter

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Received: 11 October 2022 / Accepted: 8 November 2022
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Abstract
The growing market demand for semiconductor chips designed to address new and emerging applications (especially in the power device market) are driving the need for single wafer high current implanters with a much broader energy range than traditional implant space, which is primarily designed around logic and memory high dose implant requirements. This paper describes the design and capabilities of the Purion H200™ single wafer high current implanter produced by Axcelis Technologies specifically designed to deliver high beam currents and productivity over a wide energy range from sub 10 keV to over 400 keV. We discuss the design, capabilities, and unique challenges with higher power implants and review the current applications needs being addressed by this implanter in high volume manufacturing of both silicon and silicon carbide devices.

Introduction

The strong global push to balance the ever-increasing need for higher-energy consumption in this new world driven by the Internet of Things (IOT) against the need to mitigate climate change is driving a strong demand for improving and adopting new energy efficient approaches. These include a shift toward integrating renewable energy sources, a strong pull for electrification of the automotive industry (shifting away from fossil fuels) as well as integrating new devices

Published online: 05 December 2022

focusing and shaping for e cient transport, 3. Magnetic scanner to enable independent control of beam uniformity without compromising the localized angular distributions across the wafer diameter, and 4. An S-bend corrector magnet that enables independent control of average beam direction and beam parallelism across the width of the scanned region. The beamline components described above along with the source and gas box are confined within a high-voltage terminal). Since the energy of the transported beam

get lower $\sim$5–20% as the transport e ciency through the beamline becomes a limiting factor. Even though the maximum beam currents are available at $>$100 keV, wafer cooling requirements typically limit the maximum usable beam currents.

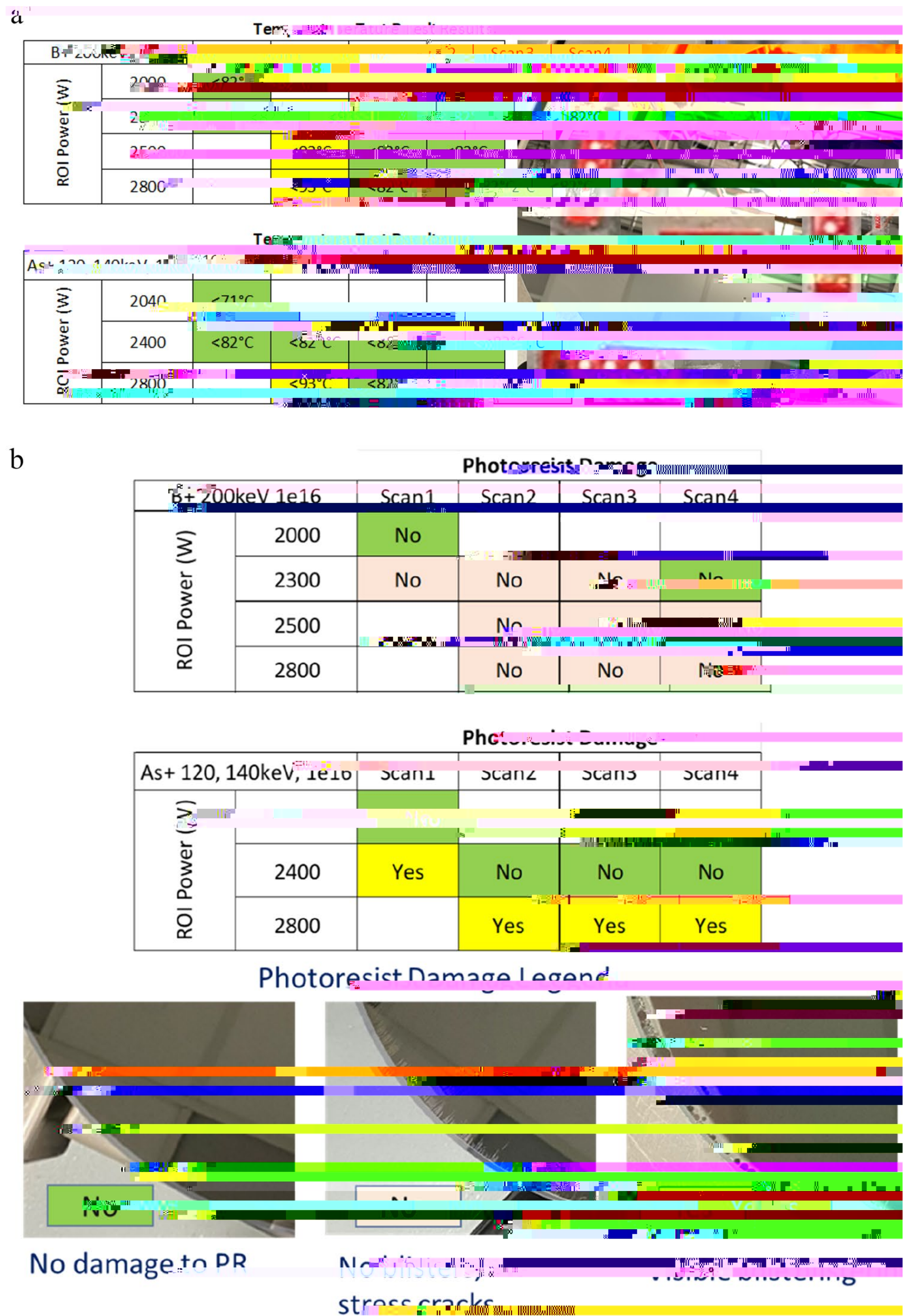

Fig. 2 **a** Results from temperature dot testing on wafers implanted with Boron or Arsenic beams with 1e16at/cm2 dose indicating the impact of various scan conditions on max temperature across the wafer (among all 5 temp dots). Photograph on the right shows the location of the temperature dot stickers on the wafer for As 2400-W implant as a sample (all tests were done similarly). Inserts are zoomed in images of the temp dot stickers that show that the 71-C dot was discolored, but 82-C dots were not confirming the temperature did not exceed 82 C on any of the locations tested on the wafer. Yellow highlighted cells in the summary table to the left indicate partial discoloration of the 93-C temp dot, while green highlight indicates no visible change. **b** Summary of Photoresist damage studies for under various beam power conditions for 1e16 B + and As + implants showing the value of optimizing the scan settings to prevent damage to the photoresist (observed near wafer edges). Important to note that the radial stress cracks may be an artifact of the blanket (unpatterned) photoresist layers

the excellent dose and uniformity control capability of the Purion H200.

Silicon carbide (SiC) option

The Purion H200 with SiC option offers the ability to process SiC wafers both at 150-mm and 200-mm wafer sizes. The SiC option integrates capabilities needed in doping SiC substrates including a source solution for Aluminum implantation, capability for heated implants for up to 650 °C wafer temperature, and reliable wafer handling for SiC wafers proven in several high-volume manufacturing fabs. The aluminum source utilizes a low temperature vaporizer with in situ CleanFlow technology that delivers high beam currents for typical dopants for SiC devices (7-mA Al^+, 20-mA N^+, 35-mA P^+, refer Fig. 1b). The Purion H200 tool with the SiC option also comes with an integrated preheat station and heated wafer clamp capabilities to deliver high

productivity for bottleneck implants (especially high-dose Al, P, and N) in the SiC MOSFET manufacturing flows.

Available for 300-mm/200-mm/150-mm wafer sizes

The Purion H200 is o ered in both 300-mm and 200-mm wafer sizes for Silicon substrates and in 150-mm and 200-mm wafer sizes for SiC substrates leveraging Axcelis' common wafer handling platform.

Applications space served by the Purion H200

The Purion H200 covers all medium (1e13 at/cm2) to high dose (typically up to 1e16 at/cm2 but extendable to 1e17 at/cm2 doses) implant applications from 10 keV up to 230 keV (and up to 460 keV with + +) implant energies and thus valu-

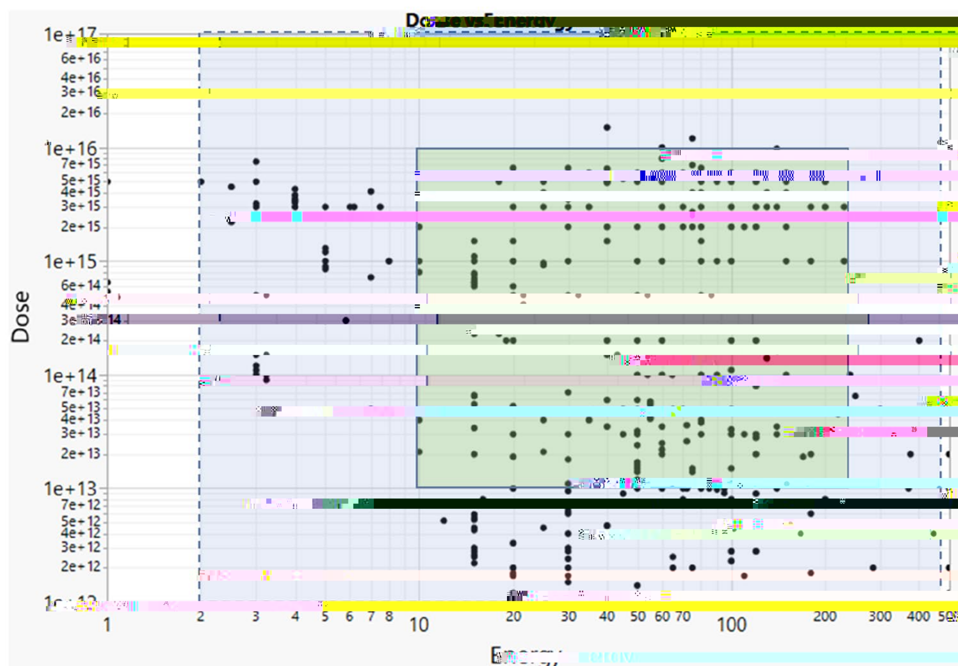

Fig. 4 Application space covered by the Purion H200 implanters. The green (inner) box represents typical operating space, while the blue (outer) box shows the extended capabilities of the tool. Dots represent various implant conditions used in power, analog, bipolar, mature, and BCD device manufacturing applications

application spaces to develop novel technology solutions for the future. To this goal, Axcelis Technologies has launched a new single-wafer high-current tool capable of covering the high- and medium-dose applications across a broad energy range from < 10 keV to > 200 keV (Single charge) for both Silicon and SiC device manufacturing. The Purion H200 tools are already integrated and qualified in leading power device manufacturing fabs for both device types and are opening up new implant applications with the wide process window that it covers.

Acknowledgments The Purion H200 project was developed with critical support from various teams at Axcelis as well as with valuable inputs from the technology and production teams at leading power device manufacturers. Special thanks to R. Rathmell, B. Vanderberg, E. Eisner, N. Colvin, N. Bassom, J. David, J. Ferrara, K. Issakimuthu, R. Reece, B. Bintz, P. Lustiber, and their teams along with the key customer account teams for their contributions to bring this product to market.

Funding Furthermore, we confirm that no funds, grants, or other support were received from outside Axcelis.

Data availability The datasets generated and mentioned in the paper are available from the corresponding author on reasonable request.

Declarations

Conflict of interest On behalf of all authors, the corresponding author states that there is no conflict of interest.

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